Medium Frequency Physical Vapor Deposited Al_2O_3 and SiO_2 as Etch-Stop-Layers for Amorphous Indium-Gallium-Zinc-Oxide Thin-Film-Transistors

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In this work, we report on amorphous-Indium-Gallium-Zinc-Oxide (a-IGZO) thin-film transistor (TFT) with medium frequency physical vapor deposited (mf-PVD) etch-stop-layer (ESL). TFT with mf-PVD ESL show comparable characteristics such as field-effect mobility (μ_{FE}), sub-threshold slope (SS^{-1}) and current ratio ($I_{ON/OFF}$) to the conventional plasma enhanced chemical vapor deposition (PECVD) ESL based TFT, however significant differences were observed in gate bias-stress stabilities. The TFTs with mf-PVD ESL showed lower threshold-voltage (V_{TH}) shifts compared to TFTs with PECVD ESL when stressed under a gate field of +/−1 MV/cm for duration of 10^4 seconds in dark and light conditions. We associate the better bias-stress stability of the mf-PVD ESL based TFT to better passivating properties and the low hydrogen content of the mf-PVD layer compared to PECVD layer.
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Amorphous oxide semiconductors (AOSs) are gaining traction to replace the a:SiH in TFTs applied in liquid crystal display (LCD) and organic light-emitting diode display (OLED) backplanes. These oxide semiconductor have high transparency and relatively high electron mobility in the amorphous state. An additional advantage lies in the low process temperature required for AOS integration on plastic film and so potentially enabling flexible transparent display and electronics. Among many AOSs, a-IGZO is the most promising due to its high mobility, excellent uniformity, and the compatibility with transparent and flexible substrate, as compared to conventional amorphous and polycrystalline silicon.[1–8] For either LCD or OLED displays with IGZO backplane, bottom-gate top-contact (BGTC) ESL configuration is preferred. The ESL protects the a-IGZO back channel from damages caused during the source-drain metallization and patterning.[9–11] The damage-free surface improves the bias stabilities especially at accelerated bias stress conditions under illumination. However commonly the ESL is deposited by plasma assisted CVD processes to which a-IGZO can be sensitive.[12] Therefore there is a need to investigate the effect of the ESL on the characteristics of a-IGZO TFTs.

PECVD based SiO_2 deposited at temperature higher than 350°C using SiH_4/N_2O chemistry is commonly used as an ESL in Flat-Panel-Display (FPD) industry due to its fast deposition rate, high uniformity and good step coverage. For the integration on commercialized flexible substrates like PEN or polyimide, deposition and process temperature should be lower to prevent shrinkage of the plastic foil and allow easy de-lamination. It is known that PECVD layer deposited at lower temperature deteriorate layer quality leading to lower density, higher amount of dangling bonds and an increase in the amount of hydrogen incorporated into the SiO_2 layer. The poor density and increase of hydrogen is problematic for a-IGZO TFTs because it leads to uncontrolled doping density.[13–14] Few research groups have demonstrated the use of PVD based dielectrics (SiO_2 and Al_2O_3) as passivation layer or ESL as an alternative to PECVD layer which has the doping issue with a-IGZO.[15,16,22] Despite the fact that PVD dielectrics intrinsically contain less hydrogen, parameters such as deposition rates, uniformity, defect density and electrical properties like leakage current and breakdown voltage are often insufficient to meet the manufacturing requirements of the industry. Recently mf-PVD Al_2O_3 layers have been demonstrated with high deposition rate and sufficient uniformity up to Gen-8 size.[17] This might allow to replace the conventional PECVD SiO_2 layer to achieve better TFT characteristics. In this paper, we realized IGZO-TFTs with different mf-PVD ESL (SiO_2 and Al_2O_3) and compared them to conventional PECVD SiO_2 ESL based TFTs.

Experimental

All TFT were made on conducting silicon substrate with thermal SiO_2 (120 nm) as gate dielectric and the Si substrate was used as a common gate electrode. The use of high-quality high-temperature thermal SiO_2 guarantees that none of the observed bias instabilities is related to the gate dielectric (GD) layer. In the first step, a-IGZO layer was deposited by dc sputtering at room temperature (RT) using a-IGZO target (In : Ga : Zn = 1 : 1 : 1 atomic%) using a Ar/ O_2 mixture. Following the a-IGZO deposition, three different kinds of etch-stop-layers of equal thickness were deposited on three different samples i.e. two layers were deposited by mf-PVD (50 kHz) of Si and Al at room temperature with Ar/O_2 mixture and one by PECVD at 200°C with SiH_4/N_2O chemistry. In the next step the ESL/a-IGZO stack was patterned by dry etch and wet etch followed by contact opening by dry etch. The Mo S/D contacts were formed by molybdenum (Mo) sputtering and dry etch. All layers were patterned by standard photolithography. In the last step all the samples were subjected to thermal annealing at 250°C in N_2 ambient for 1 hr. The electrical properties of a-IGZO TFTs were measured using an Agilent 4156 parameter analyzer in N_2 environment. The characteristics of the ESL were measured by the ellipsometry and electrical characterization techniques. Relative layer density was characterized with standard BHF (1:50 with H_2O) wet etch rate and hydrogen % was characterized by Elastic-Recoil-Detection (ERD) technique.

Results and Discussion

The use of high quality thermally grown SiO_2 as gate-dielectric assures that any variations in TFT characteristics and the bias-stress stabilities are most likely related to the ESL. Fig. 1 shows a schematic cross-section of the a-IGZO TFTs. Fig. 2(a) and 2(b) shows typical transfer (I_{DS} -V_{GS}) and output (I_{DS} –V_{DS}) characteristics of three TFTs. As listed in Table I, for TFTs with mf-PVD ESLs the characteristics such as μ_{FE}, SS^{-1} and $I_{ON/OFF}$ ratio are between 15–17 cm^2/V.s, 0.20–0.30 V/decade and $< 10^7$ respectively. TFT with PECVD SiO_2 ESL in comparison has a substantially lower μ_{FE} of 10–12 cm^2/V.s; while the other parameters are comparable to the TFT with mf-PVD ESL.

In case of the PECVD based ESL, the impact of the deposition temperature on the TFT characteristics cannot be completely decoupled

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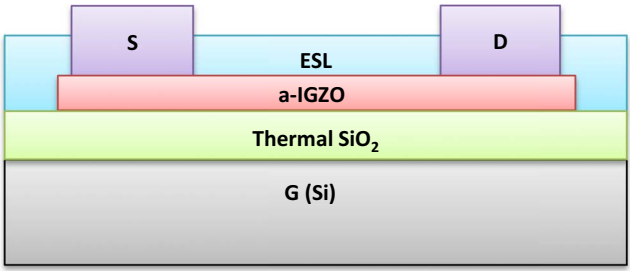

Figure 1. Cross-section of ESL configuration based a-IGZO TFTs.

between the change in SiO_2 quality and the impact of the temperature on the a-IGZO. The low deposition temperature (<250°C) of PECVD SiO_2 ESLs lead to increase in hydrogen content, decrease in the density and corresponding poorer electrical performance. Several research groups have reported that hydrogen atoms produced by SiH_4 plasma diffuse fast in the a-IGZO layer, creating a shallow electron donor level.[18] On the other hand, oxygen atoms in N_2O plasma were inclined to oxidize the a-IGZO layer surface, which decreased the carrier concentration of a-IGZO layers.[19] An optimized H_2 and O_2 plasma ratio layer can lead to improved transistor characteristics. In case of mf-PVD layers, optimized sputter plasma (O_2 to Ar ratio) tends to cause less impact on the a-IGZO below. In this case, because no hydrogen source is present, changes in TFT characteristics related to hydrogen doping can be ruled out with exemption to the PECVD SiO_2. The Ar rich plasma can change the a-IGZO layer from semiconducting to conducting by changing the ratio of metal atoms (Ga, In and Zn) and the O_2 rich plasma can cause the surface oxidation leading to more resistive layer and therefore both can influence the TFT characteristics. In fact it is reported that the Ar plasma treated surface has relatively higher In and relatively lower Ga and Zn due to the difference of the sputtering yield of these atoms.[20] However, these differences are reduced after an annealing step. In case of TFT with mf-PVD ESLs, high mobility and negative V_{TH} could be due to the change in the conductivity of the channel at the ESL interface. It could also be possible that the longer or higher temperature anneal conditions are required for mf-PVD ESL based TFTs to have similar properties like PECVD ESL based TFT. In further TFT characterizations, i.e. the bias-stress stabilities in dark conditions as shown in Fig. 3 under positive bias-stress (PBS) and negative bias-stress (NBS) of +/−1 MV/cm field for a duration of 10^4 seconds; it is observed that the TFTs with mf-PVD (SiO_2 and Al_2O_3) ESL exhibited lower V_{TH} shift of less than +/−0.5 V in comparison V_{TH} shift of more than +/− 2.0 V for PECVD ESL TFTs. Furthermore, quite similar to the large shifts in dark conditions in negative direction, large shifts are observed under light conditions as shown in Fig. 4 i.e. negative bias illumination stress (NBIS) condition of −1 MV/cm field for duration of 10^4 seconds under light source of 425 nm (2.92 eV) wavelength with photon flux of 10^{16} $cm^{-2}s^{-1}$. The mf-PVD ESL (SiO_2 and Al_2O_3) TFTs show lower degradation of less than −3.0 V shift compared to −7.1 V shift in case of PECVD SiO_2 ESL TFTs. To understand more on these characteristics differences, all the three layers were characterized. The properties of the individual ESLs are listed in Table II. It is clearly understood that PECVD SiO_2 layer's based TFTs

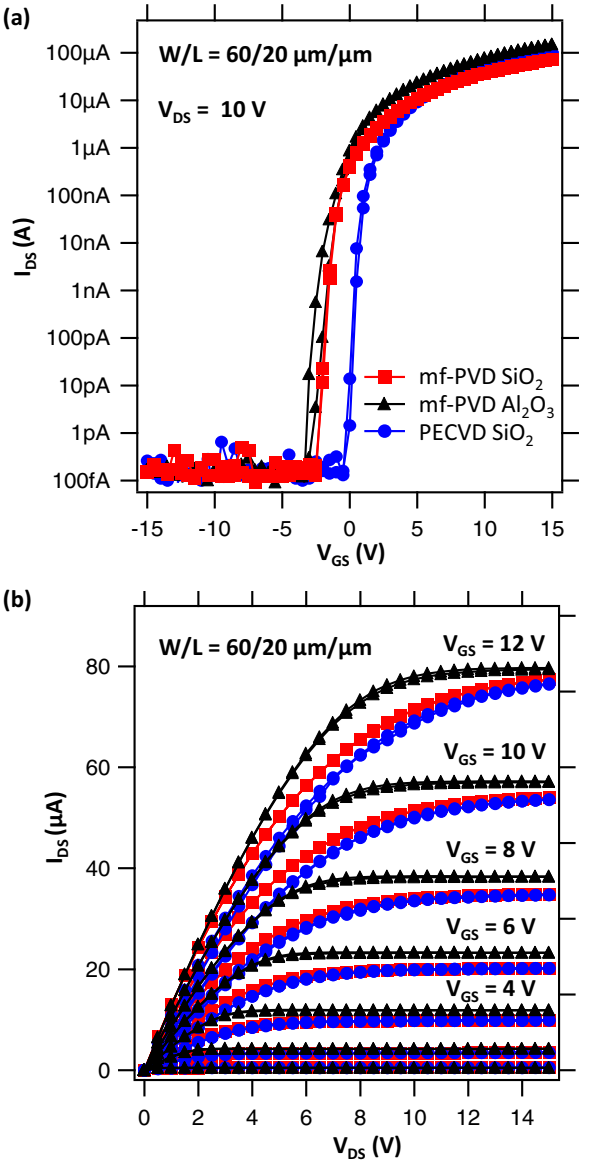

Figure 2. (a) Transfer (V_{GS}-I_{DS}) and (b) output (V_{DS}-I_{DS}) characteristics of TFTs with mf-PVD SiO_2, mf-PVD Al_2O_3 and PECVD SiO_2 ESL's with W/L = 60/20 µm/µm.

are poor in characteristics as the layers properties such as density and dielectric constant are far off compared to ideal layer characteristics.[22] In addition Fig. 5 showed the ERD characterization data of each ESL. The ERD analysis was performed with the conditions of 8.0 MeV energy with Cl^{4+} element at a scattering angle of 39° and sample tilt of 20°. Also large irradiated area (0.5 cm^2) taken to minimize changes of the initial profiles during the measurement. The estimated absolute uncertainties on the reported values are ∼ 0.5 at.%. From the graph

Table I. Comparison of TFT parameters for the three different types of ESLs.

TFT Parameters	ESL RT mf-PVD SiO_2	ESL RT mf-PVD Al_2O_3	ESL 200°C PECVD SiO_2
μ_{FE} Range (cm^2/(V.s)	15–17	15–17	10–12
SS^{-1} Range (V/dec)	0.2–0.3	0.2–0.3	0.2–0.3
V_{ON} Range (V)	−(0.5–3.0)	−(0.5–4.0)	−(0.1– 2.5)
Hysteresis (V)	<0.1	<0.1	<0.1
I_{OFF} (pA)	<1.0	<1.0	<1.0
NBS & PBS (V)	<1.0	<1.0	>1.5
NBIS (V)	<2.0	<2.0	>6.0

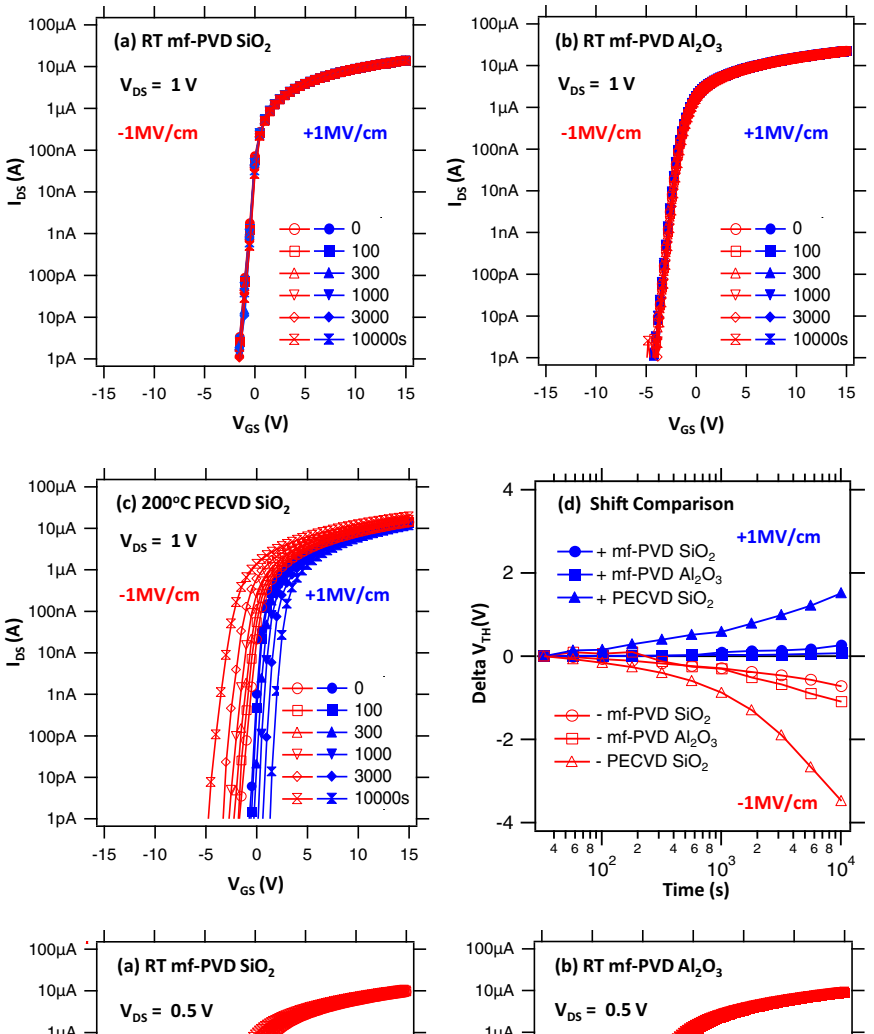

Figure 3. Transfer characteristics (V_{GS}-I_{DS}) of a-IGZO TFT (W/L = 60/20 μm/μm) as function of duration time at 1MV/cm field in positive and negative gate bias stress direction for TFT with (a) mf-PVD SiO_2, (b) mf-PVD Al_2O_3 and (c) PECVD SiO_2. (d) V_{TH} shift of all a-IGZO TFTs as a function of stress time.

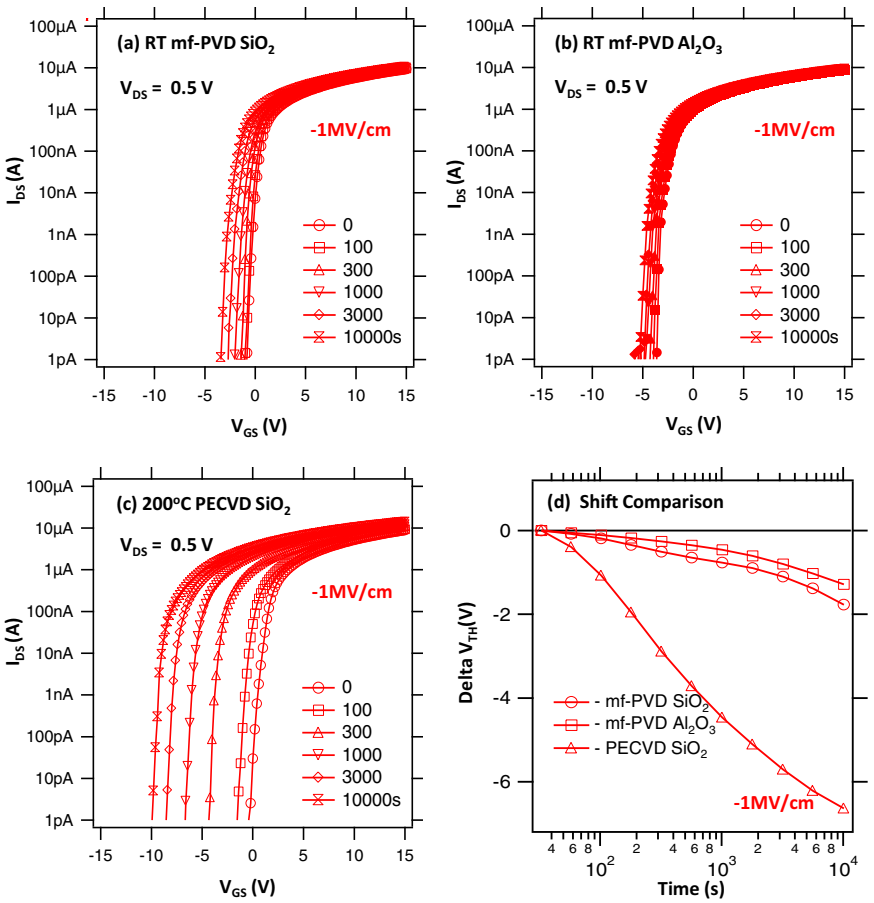

Figure 4. Transfer characteristics (V_{GS}-I_{DS}) of a-IGZO TFT (W/L = 60/20 μm/μm) as function of duration time at −1MV/cm field under light for TFTs with (a) mf-PVD SiO_2, (b) mf-PVD Al_2O_3 and (c) PECVD SiO_2. (d) V_{TH} shift of all a-IGZO TFTs as a function of stress time.

Table II. Properties comparison of the mf-PVD SiO_2, mf-PVD Al_2O_3 and PECVD SiO_2 layers.

SiO_2 Parameters	RT mf-PVD SiO_2	RT mf-PVD Al_2O_3	200°C PECVD SiO_2
Deposition Rate (nm)	Medium	Medium	High
Etch Rate in 8% BHF (nm)	33	37	112
Breakdown (MV/cm)	8	7	5.9
Hydrogen Content (%)	1	2.91	6.4
Dielectric Constant	3.9	8	5.7
Leakage @ 2MV/cm (mA/cm^2)	$\approx 5e^{-5}$	$\approx 4e^{-5}$	$\approx 2e^{-4}$

it is clear that the PECVD SiO_2 layer's hydrogen content is 6.43 at.% which is much higher than 1.01 at. % of mf-PVD SiO_2 layer and 2.8 at.% of mf-PVD Al_2O_3 layer.

In bias stress experiments in the dark (NBS and PBS) and under light (NBIS) conditions, the change at back channel interface due to the ESL deposition dominate the V_{TH} shift. Not much is reported on these stress stabilities for PVD ESL based TFTs. In few publications where PVD layer (SiO_2 and Al_2O_3) is used as passivation layer[15–16] or as dopant blocking layer,[21] little explanation around the NBS and PBS is provided. In our previous work; we compared the mf-PVD SiO_2 ESL based TFT characteristics and their bias-stress stabilities (PBS and NBS) to high temperature (300°C) PECVD SiO_2 and low temperature (200°C) SiO_2 ESL based TFTs.[22] We observed that high temperature PECVD SiO_2 ESL and mf-PVD SiO_2 ESL based TFTs show comparable characteristics. Here we extended our work with the addition of mf-PVD Al_2O_3 ESL TFT characteristics and their bias-stress stabilities (NBS and PBS) data. In addition NBIS data for all the ESL stacks (PECVD SiO_2, mf-PVD SiO_2 and mf-PVD Al_2O_3) have been elaborated on. In PBS as the TFT operate in fully on mode, only the front interface (a-IGZO/gate dielectric) is important. However the positive V_{TH} shift can be explained by assuming oxygen adsorption on the back surface of the active layer which decreases the concentration of free electrons in the channel layer.[23] A passivation layer (ESL in this case) which isolates the channel layer from the environment prevents oxygen adsorption effectively, and thus solves the problem. The 200°C PECVD layer has extremely high etch rate as listed in Table II, this mean that the layer is poor in density; could have lots of pin holes and thus poor for the passivation for O_2 and water. So oxygen adsorptions at the back interface resulted to large positive shifts. In NBS, the TFT works in depletion mode both the interfaces (a-IGZO/thermal SiO_2 and a-IGZO/ESL) are active, however the impact of the front interface (a-IGZO/thermal SiO_2) will be much lower or negligible and also similar to PVD ESL case. So on a similar note as in the PBS case the back interface change dominates the shift in NBS as well, the external humidity and other gas molecules can thus permeate through

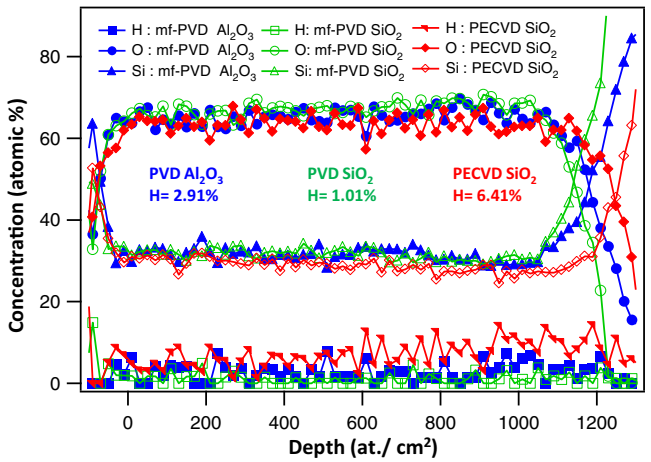

Figure 5. ERD comparison of mf-PVD SiO_2, mf-PVD Al_2O_3 and PECVD SiO_2 layers.

these empty regions of poor passivation. Moisture reaching the a-IGZO layer enhances the generation of shallow donor states created by visible light radiation and thus induces an increase in carrier density within a-IGZO. This enhances the conductivity and so reflects in large negative shifts under bias conditions. Other possible explanation is the peak hydrogen concentration which varies opposite to deposition temperature in PECVD processes i.e. layers at 200°C will contains higher hydrogen than that of layers athigher temperature. These results support the conjecture that a significant amount of hydrogen must have been incorporated for low temperature layers case. Hydrogen is well known to contribute shallow donor states to a-IGZO, which increases their electrical conductivity. It is very probable that the incorporation of hydrogen has generated donor states within the a-IGZO bulk, hence inducing a large –ve shift due to the additional carriers. Over all in both the PBS and the NBS cases, the difference in the amount of the V_{TH} shift originate from the difference in bond structure at the a-IGZO/ESL interface. The deposition temperature of SiO_2 has a strong influence on both the microstructure of SiO_2 and the a-IGZO/SiO_2 interface bonding state. The silicon oxide layer when deposited at a higher temperature (>300°C) much stronger bonds could be formed at the interface.[22,24] The quality of the a-IGZO/SiO_2 interface is conjectured to determine the V_{TH} shift of all TFTs in bias tests. Reported higher temperature (deposited >300°C) PECVD ESLs or passivation and dual layer passivation layers stacks due to their much better passivating properties do not show similar kind of large PBS and NBS shifts.[25–26] Quite similar to NBS explanation, the back channel interface change produces a substantial instability under NBIS. It is reported that the back channel interface exhibits a high-density of near valence-band-maximum (VBM) states caused by oxygen vacancies (V_O), which generate holes by photo-exciting electrons to the conduction band when illuminated.[27–28] The holes then diffuse to the interface of the gate dielectric by the assistance of the negative bias stress. Post a-IGZO process integration steps affect these back channel interface VBM states. ESL and passivation layers are used to prevent these back surface changes, however, the deposition conditions of those layers also impact the VBM states. The amount of oxygen, hydrogen and water molecules, which are present in these layers, become very important. It is also mentioned that increasing the amount of incorporated hydrogen (occurring during PECVD ESL deposition) increases the NBIS related instability due to formation of a hydrogen-related complex[29–30] and incorporated O_2 (possible in case of PVD ESL) in a-IGZO reduces the deep traps caused due to oxygen vacancy related defects.[31] In summary, PVD SiO_2 is deposited in oxygen rich plasma and this reduces the deep trap states close to the back surface. PECVD SiO_2 doesn't oxidize a-IGZO, but introduces interstitial hydrogen into the material which doesn't reduce the deep trap states and involve in large V_{TH} shifts. To counter this some groups established N_2O plasma treatment to back a-IGZO surface prior to PECVD SiO_2 deposition. This treatment oxidizes the top surface of the IGZO and reduces the diffusion of H_2 in the following SiH_4 gas step. The result of back interface change in case of N_2O plasma is very much similar in PVD ESL deposition case.[24,26] We also extracted the traps for all the three different type of TFTs with NBIS data from the equation: Trap Charges = $(\Delta V_{TH}{}^* C_{ox})$; where $C_{ox} = (K_{SiO}{}^* K_o) / (X_{ox})$ cm^{-2}, where ΔV_{TH} is voltage shift under NBIS, $K_{SiO} = 3.9$ for SiO_2, $K_o = 8.854e^{-12}$ F/m, X_{ox} is the thickness of dielectric. With the assumption of uniform distribution

the above calculated charges were divided by thickness of a-IGZO. It is observed that the numbers for the PECVD SiO_2 layer's TFTs were much higher i.e. 1.5 e^{18} cm^{-3} than in case of PVD layer case TFTs i.e. 4.50 e^{17} cm^{-3} in PVD SiO_2 TFTs and 3.00 e^{17} cm^{-3} in PVD Al_2O_3 TFTs. Overall the lower hydrogen content of mf-PVD layer and its better passivating properties could be the reasons behind better bias-stress stabilities of mf-PVD ESL based TFTs but parameters such as layer's density, dielectric constant and leakage, which correspond to the number of defects and the dangling bonds, can also influence the TFT characteristics. Further if we assumed that increased trapping due to higher defect density of the ESL would be the main issue, the improvement in bias-stress stability with PVD ESL should mostly be visible in the negative bias-stress and not significantly influence the positive bias-stress. As we see improvement in both positive and negative bias-stress stability (under dark), which is more in-line with changes in the bulk properties of a-IGZO with mf-PVD layer as ESL.

Conclusions

In summary, mf-PVD SiO_2 and mf-PVD Al_2O_3 ESL based a-IGZO TFTs has been realized. In comparison to the conventional PECVD SiO_2 ESL based TFTs, the TFTs with mf-PVD (SiO_2 and Al_2O_3) ESL exhibited better bias-stress stabilities under dark and light conditions. Better passivation properties and the lower hydrogen content of mf-PVD (SiO_2 and Al_2O_3) layers has been identified as the major cause of this difference.

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References

1. T. Kamiya, K. Nomura, and H. Hosono, *Sci. Technol. Adv. Mater.* **11**, 044305 (2010).
2. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Nature*, **432**, 488 (2004).
3. J. S. Park, W. -J. Maeng, H. -S. Kim, and J. -S. Park, *Thin Solid Films* **520**(6), 1679 (2012).
4. P. Barquinha, L. Pereira, G. Gonçalves, R. Martins, and E. Fortunato, *J. Electrochem. Soc.*, **156**(3), H161 (2009).
5. H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono,*Appl. Phys. Lett.* **89**, 112123 (2006).
6. J. K. Jeong, J. H. Jeong, H. W. Yang, J. -S. Park, Y. -G. Mo, and H. D. Kim, *Appl. Phys. Lett.* **91**, 113505 (2007).
7. M. Nag, A. Chasin, M. Rockele, S. Steudel, K. Myny, A. Bhoolokam, J. Genoe, K. Myny, A. Tripathi, B. van der Putten, A. Kumar, J. -L. van der Steen, F. Li, J. Maas, E. van Veenendaa, G. Gelinck, and P. Heremans, *Journal of the Society for Information Display*, **21**(3), 129 (2013).
8. M. Nag, M. Rockele, S. Steudel, A. Chasin, K. Myny, A. Bhoolokam, M. Willegems, S. Smout, P. Vicca, M. Ameys, T. H. Ke, S. Schols, J. Genoe, J. -L. van der Steen, G. Groeseneken, and P. Heremans, *Journal of the Society for Information Display*, **21**(9), 369 (2013).
9. J. S. Jung, K. -H. Lee, K. S. Son, J. S. Park, T. S. Kim, J. H. Seo, J. -H. Jeon, M. -P Hong, J. -Y. Kwon, B. Koo, and S. Lee, *Electrochem. Solid State Lett.*, **13**(11), H376 (2010).
10. M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. -S. Park, J. K. Jeong, Y. -G. Mo, and H. D. Kim, *Appl. Phys. Lett.*, **90**(21), 212 114-1-212 114-3 (2007).
11. X. Li, E. Xin, L. Chen, J. Shi, and J. Zhang, *AIP Advances*, **3**, 032137 (2013).
12. K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono; *Appl. Phys. Lett.*, **99**, 093507-1 - 3 (2011).
13. B. S. Park, D. K. Yim, S. -M Cho, S. Y. Choi, and J. M. White, *ECS Transactions*, **54**(1) 97 (2013).
14. T. Kamyia and H. Hosono, *ECS Transactions*, **54**(1) 103 (2013).
15. J. Li, F. Zhou, H. -P. Lin, W. -Q. Zhu, J. -H. Zhang, X. -Y. Jiang, and Z. -L. Zhang, *Vacuum*, **86**(12), 1840 (2012).
16. T. Arai, N. Morosawa, K. Tokunaga, Y. Terai, E. Fukumoto, T. Fujimori, T. Nakayama, T. Yamaguchi, and T. Sasaoka, *SID Int. Symp. Dig. Tech. Pap.* **41** 1033 (2010).
17. A. Kloeppel, J. Liu, and E. Scheer, *SID Symp. Dig. Tech. Pap.*, **44**(1), 647 (2013).
18. J. Kim, S. Bang, S. Lee, S. Shin, J. Park, H. Seo, and H. Jeon, *Journal of Materials Research*, **27**(17), 2318 (2012).
19. D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park, and J. Chung, *Appl. Phys. Lett.* **90**, 192101 (2007).
20. J. -S. Park, J. K. Jeong, Y. -G. Mo, H. D. Kim, and S. -I. Kim, *Applied Physics Letters* **90**, 262106 (2007).
21. R. Hayashi, A. Sato, M. Ofuji, K. Abe, H. Yabuta, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, *Improved Amorphous In-Ga-Zn-O TFTs. SID Symposium Digest of Technical Papers*, **39**, 621 (2008).
22. M. Nag, S. Steudel, A. Bhoolokam, A. Chasin, M. Rockele, K. Myny, J. Maas, T. Fritz, J. Trube, G. Groeseneken, and P. Heremans, *Journal of the Society for Information Display*, **22**(1), 23 (2014).
23. J. K. Jeong, J. K. Jeong, H. W. Yang, J. H. Jeong, Y. -G. Mo, and H. D. Kim, *Appl. Phys. Lett.* **93**, 123508 (2008).
24. H. Hayashi, Y. Nakazaki, T. Izumi, A. Sasaki, T. Nakamura, E. Takeda, T. Saitoh, M. Goto, and H. Takezawa, *SID Symp. Dig. Tech. Pap.*, **45**(1), 853 (2014).
25. J. S. Jung, K. -H. Lee, K. S. Son, J. S. Park, T. S. Kim, J. H. Seo, J. -H. Jeon, M. –P. Hong, J. -Y. Kwon, B. Koo, and S. Lee, *Electrochemical and Solid-State Letters*, **13**(11) H376 (2010).
26. B. S. Park, D. K. Yim, S. -M. Cho, S. Y. Choi, and J. M. White, *ECS Transactions*, **54** (1) 97 (2013).
27. K. Nomura, T. Kamiya, and H. Hosono, *Appl. Phys. Lett*, **99**(5), 053505 (2011).
28. B. Ryu, H. K. Noh, E. A. Choi, and K. J. Chang, *Appl. Phys. Lett*, **97**(2), 022108 (2010).
29. H. K. Noh, J. S. Park, and K. J. Chang, *Journal of Applied Physics*, **113**(6), 063712 (2013).
30. H. J. Kim, S. Y. Park, H. Y. Jung, B. G. Son, C. -K. Lee, C. –K. Lee, J. H. Jeong, Y. -G. Mo, K. S. Son, M. K. Ryu, S. Lee, and J. K. Jeong, *J. Phys. D: Appl. Phys*, **46**(5), 055104 (2012).
31. K. H. Ji, J. -I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim, C. S. Hwang, D. Lee, H. Hwang, and J. K. Jeong, *Appl. Phys. Lett.* **98**(10), 103509 (2011).